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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/802,253	03/17/2004	Chiou-Feng Chen	A-75031	4330

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EDWARD S. WRIGHT
1100 ALMA STREET, SUITE 207
MENLO PARK, CA 94025

EXAMINER	
NGUYEN, HIEN N	
ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 07/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

4-A

Office Action Summary	Application No.	Applicant(s)	
	10/802,253	CHEN ET AL.	
	Examiner	Art Unit	
	Hien N. Nguyen	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *the Election Response filed on 5/18/05*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) *12 and 23* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 13-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 March 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/25/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Search Report*.

DETAILED ACTION

1. The amendment filed on 5/18/05 for NOT canceling the non-elected claims (Group II) is found non-responsive (MPEP § 821.03). Therefore, claims 12 and 23 **are withdrawn** from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Group II, there being no allowable generic or linking claim. Election was assumed **without** traverse in the reply filed on 5/18/05.

2. Claims 1-11 and 13-22 are presented for examining.

Double Patenting

Claims 1-11 and 13-22 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-30 of copending Application No. 10/803,183. Although the conflicting claims are not identical, they are not patentably distinct from each other because the bit line diffusion and the common source region (as recited in claims 1-11 and 13-22 of the present application) are obviously spaced apart from each other toward opposite sides of the active area as recited in claims 1-30 of application 10/803,103.

More **specifically** for example:

Application 10/802,253
1. A flash memory cell array, comprising: a substrate having an active area, a plurality of vertically stacked pairs of floating gates and control gates arranged in rows **above the active area**, with the control gates being positioned above and aligned with the floating gates, select and erase gates aligned with and positioned on opposite sides of each of the stacked gates, a bit line above each row, bit line diffusions in the active area between and partially overlapped by two select gates, **a bit line contact interconnecting the bit line and the bit line diffusions in each row, and a common source region in the active area beneath** the erase gate and partially overlapped by the floating gates.

Application 10/803183
1. A NAND flash memory cell array, comprising: a substrate having an active area, a bit line diffusion and a source region spaced apart from each other toward opposite sides of the active area, a plurality of vertically stacked pairs of floating gates and control gates **arranged in a row between the bit line diffusion and the source region**, with the control gates being positioned above and aligned with the floating gates, a select gate and an erase gates aligned with and positioned on opposite sides of each of the stacked gates, with select gates at the ends of the row partially overlapping the bit line diffusion and the source region, a diffusion region in the active area beneath each of the erase gates, a bit line above the row, and a bit line contact interconnecting the bit line and the bit line diffusion.

Regarding independent claim 1, an argument of inherency exists as follows: the bit line diffusion and the source region as recited in claim 1 (10/803,183 and highlighted above) is **actually** the active area as recited in claim 1 of the present application. Furthermore, even though claim 1 of 10/803,183 has not specifically recited that the floating gate and the control gate are arranged **above the active area**, it is known in the art of Flash memory that the gates (floating and control) must be above the active area (i.e. the source region).

Application 10/802,253
13. A flash memory cell, comprising: a substrate having an active area, a . vedically stacked pairs of floating gate and control gate above the active area, with the control gate being positioned above and aligned with the floating gate, select and erase gates aligned .with and positioned on opposite sides of the stacked gates, a source region in the active area underneath the erase gate and padially overlapped by the floating gate, **a bit line extending above the gates**, a bit line diffusion in the active area partially overlapped by the select gate, and a bit line contact interconnecting the bit line and the bit line diffusion.

Application 10/803183
1. A NAND flash memory cell array, comprising: a substrate having an active area, a bit line diffusion and a source region spaced apart from each other toward opposite sides of the active area, a plurality of vertically stacked pairs of floating gates and control gates **arranged in a row between the bit line diffusion and the source region**, with the control gates being positioned above and aligned with the floating gates, a select gate and an erase gates aligned with and positioned on opposite sides of each of the stacked gates, with select gates at the ends of the row partially overlapping the bit line diffusion and the source region, a diffusion region in the active area beneath each of the erase gates, a bit line above the row, and a bit line contact interconnecting the bit line and the bit line diffusion.

Regarding independent claim 13 of the instant application, the obviousness rejection of "a bit line extending above the gates" as recited in present application is encompassed in the fact that "the floating gates and control gates arranged in a row (claim 1, line **4**, application 10/803,183) and "a bit line above the row" (claim 1, line **10**, application 10/803,183)

Regarding the dependent claims 2-11 and 14-22, an example of an argument of obvious and inherency is *illustrated as follow:*

Claim 3 of present application is

> *3. The flash memory cell array of Claim 1 wherein the control gates, select gates and erase gates surround the floating gates in a manner which provides a relatively large inter-gate capacitance for high-voltage coupling during an erase operation.*

encompassed with claim 2 (10/803,183)

Application 10/803183

2. The memory cell array of Claim 1 wherein the control gates, the select gates and the erase gates surround the floating gates in a manner which provides a relatively large inter-gate capacitance for high-voltage coupling during an erase operation.

Claim 2 of present application is

2. The flash memory cell array of Claim 1 including a relatively thin tunnel oxide between the floating gates and the substrate, a first relatively thick dielectric between the floating gates and the select and erase gates, and a second relatively thick dielectric between floating gates and control gates.

encompassed with claim 4 (10/803,183)

Application 10/803183

4. The memory cell array of Claim 1 including a relatively thin tunnel oxide between the floating gates and the substrate, and relatively thick dielectrics between the floating gates and the other gates.

Claim 6 of present application is

6. The flash memory cell array of Claim 1 wherein program paths extend from off-gate channel regions between the select gates and the floating gates to the floating gates, and high voltage is coupled to the floating gates from the control gates, the erase gates on the sides of the stacked gates, and the **common source regions.**

encompassed with claim 6 (10/803,183) since "the channel beneath the floating gate" is "the source region".

Application 10/803183

6. The memory cell array of Claim 1 wherein program paths extend from off-gate channel regions between the select gates and the floating gates to the floating gates, and high voltage is coupled to the floating gates from the control gates, from the erase gates, and from **the channel regions beneath the floating gates.**

The remaining dependent claims are rejected with the obviousness and inherency as shown in the example above.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Van Houdt (6,486,509), Hsieh (6,818,512) and Guterman et al.(6,861,700) disclose a split-gate flash memory and are cited as of interest.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hien N. Nguyen whose telephone number is (571) 272-1879. The examiner can normally be reached on Monday through Thursday 9:30 AM to 7:00 PM..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

H. Nguyen
July 22, 2005

Hien Nguyen
Patent Examiner